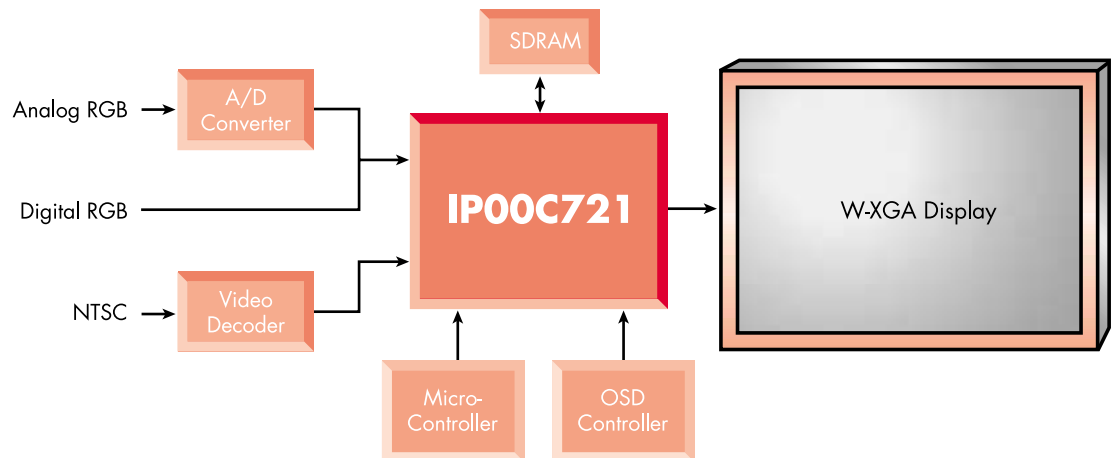# IP00C721

Image Scaling Device up to Wide-XGA

Output up to 80 Mpixels/sec., high-resolution 4x4 interpolation filter, single SDRAM device operation
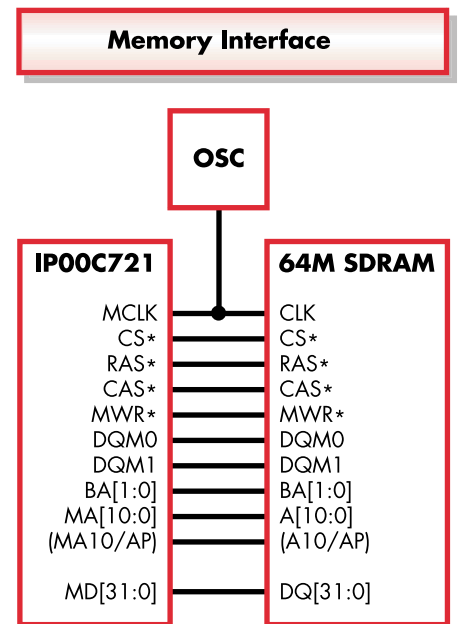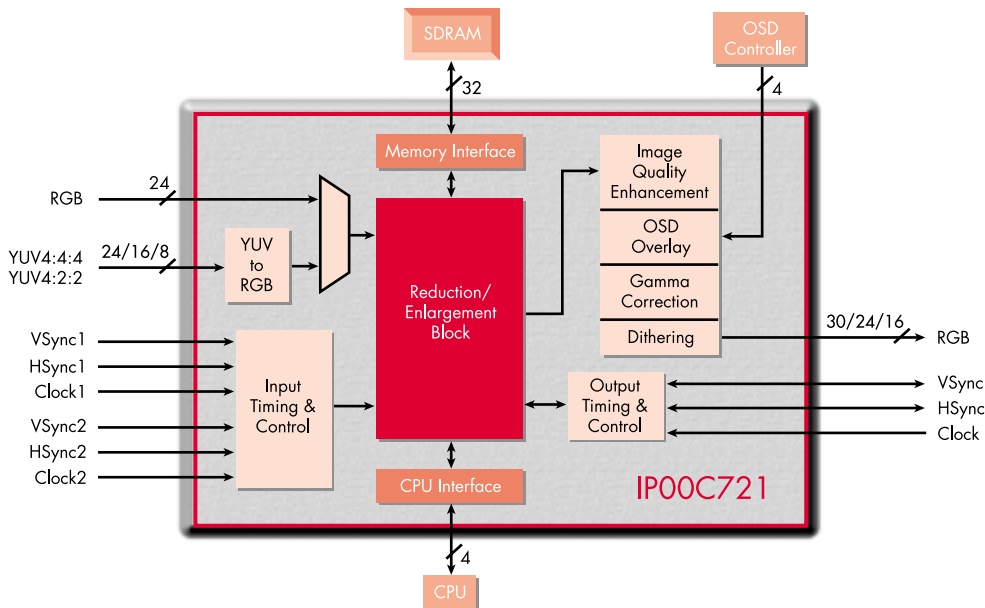
General Description

The IP00C721 is a low-cost device for real-time image resizing and frame rate conversion up to Wide-XGA resolution output. It features a 4x4 pixel interpolation core, with higher sub-pixel resolution than previous devices. The IP00C721 has 2 image input ports: 1) digital RGB 24 bits up to 108 MHz, and 2) digital YUV up to 80 MHz. The output image port can be either 24 bits or 30 bits with a maximum speed of 80 mpixels/sec, and can be driven by an internal or external pixel clock. Lower bit resolutions are also supported for 18-bit display devices. The input and output image ports are completely independent to allow simultaneous image scaling and frame rate conversion. The IP00C721 has an embedded image memory controller for direct interface to an external SDRAM device. The IP00C721 is ideally suited for applications such as projectors and low-cost display systems.

Support Tools

- Evaluation Board
- Local Technical Support

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Block Diagram labels:

SDRAM — 32
OSD Controller — 4

Memory Interface

RGB — 24
YUV4:4:4 / YUV4:2:2 — 24/16/8
YUV to RGB

VSync1, HSync1, Clock1, VSync2, HSync2, Clock2 → Input Timing & Control

Reduction/ Enlargement Block

Image Quality Enhancement
OSD Overlay
Gamma Correction
Dithering

30/24/16 → RGB

Output Timing & Control → VSync, HSync, Clock

CPU Interface — 4 — CPU

IP00C721

Memory Interface diagram:

OSC

IP00C721	64M SDRAM
MCLK	CLK
CS*	CS*
RAS*	RAS*
CAS*	CAS*
MWR*	MWR*
DQM0	DQM0
DQM1	DQM1
BA[1:0]	BA[1:0]
MA[10:0]	A[10:0]
(MA10/AP)	(A10/AP)
MD[31:0]	DQ[31:0]

IP00C721 Features

Input Image Formats

- RGB 24-bit up to 108 MHz
- YUV4:2:2 16-bit & YUV4:4:4 24-bit up to 80 MHz
- Image size up to 2400 pixels horizontally with 1438 active pixels
- External synchronization (H Sync., V Sync., Clock)
- Interlaced and progressive scan supported

Output Image Formats

- RGB (30)24-bit up to 80 MHz
- Image size up to 2048 pixels horizontally with 1438 active pixels
- External or internal synchronization modes

Scaling

- 4x4 pixels programmable interpolation
- Precision up to 1/64th of a pixel
- Independent H and V scaling ratios
- Aspect ratio conversion (non-linear scaling)

Frame Rate Conversion

- Independent sync. signals for the input and output image ports
- Frame synchronization function to avoid frame tearing

External Memory

- SDRAM (SGRAM) with 32-bit memory bus interface
- Can operate with a single memory device
- 110 MHz maximum memory clock

Other Features

- YUV-to-RGB conversion with 6 coefficients
- 16-color OSD overlay
- Color dithering for 24-bit or 18-bit output
- Edge Enhancement
- Gamma Correction LUT (8-bit in, 10-bit out)
- Brightness and Contrast adjustments
- Measurement of input signal characteristics
- Keystone correction
- LVTTL-compatible inputs and outputs

CPU Interface

- 4-line serial

Power Supply Voltage

- Two sources: 3.3V and 2.5V

Package

- 208-pin Plastic QFP

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